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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/735,806	12/16/2003	Kazunari Sesumi	740165-368	2857
22204	7590	11/29/2005	EXAMINER PRETLOW, DEMETRIUS R	
NIXON PEABODY, LLP 401 9TH STREET, NW SUITE 900 WASHINGTON, DC 20004-2128			ART UNIT 2863	PAPER NUMBER

DATE MAILED: 11/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/735,806	SESUMI, KAZUNARI
	Examiner	Art Unit
	Demetrius R. Pretlow	2863

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 16 September 2005.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) 6-10 is/are allowed.
- 6) Claim(s) 1,3-5 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 16 December 2003 is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) Notice of Informal Patent Application (PTO-152)
- 6) Other: _____

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 1,3-5 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1,3-5 are rejected under 35 U.S.C. 102(b) as being anticipated by Hayashi et al. (US 2002/0019898). Given the broadest interpretation, in reference to claim 1, Hayashi et al. teach a group of external terminal s to which a plurality of external devices can be connected; Note Figures 1, the connection to the high speed and low speed devices. Hayashi et al. teach a processor carrying out computation and control on the basis of programs; Note paragraph 11, lines 3-6. Hayashi et al. teach a bus interface specifying an external device which is to be an object of access from among the plurality of external devices on the basis of a control signal outputted from the processor, and outputting access time data instructing an access time to said external device and a request signal requesting access to said external device; Note paragraph 15, lines 4-16. Hayashi et al. does not explicitly teach a request signal requesting access to said external device however a request signal would be inherent to the device select signal.

Note paragraph 15, line 9-10. Hayahsi et al. teach a register storing the access time data outputted from the bus interface; The operating clock signals are interpreted as access time data. Note paragraph 6, lines 1-3. Hayashi et al. teach an input terminal to which is inputted, from an exterior, a wait signal which designates extension of the access time to said external device; Note paragraph 67, lines 15-17. Hayashi et al. teach an external bus controller which, in accordance with the access time data stored in the register and the request signal outputted from the bus interface, accesses said external device via the group of external terminals, and extends the access time to said external device in accordance with the wait signal inputted the input terminal. Note paragraph 39, lines 8-18. The wait signal inherently extends the access time. Note paragraph 67, lines 15-17.

Yahashi et al. does not explicitly teach wherein the external bus controller extends the access time to said external device in units of the access time which the access time data instructs, however this would be inherent to extending the access time to external device in accordance with the wait signal. Note paragraph 39, lines 8-18.

In reference to claim 3, Hayashi et al. does not explicitly teach wherein the external bus controller extends the access time to said external device by adding one of or a plurality of the access times to the access time which the access time data instructs, however this would be inherent to extending the access time to external device in accordance with the wait signal. Note paragraph 39, lines 8-18. To extend time there must some sort of increase.

In reference to claim 4, Hayashi et al. teach the external bus controller extends the access time by extending a time in which an address of said external device is outputted to said external device.

In reference to claim 5, Hayashi et al. teach wherein the external bus controller extends the access time by extending a time in which a selection signal, which instructs that said external device be selected, is outputted to said external device. Note paragraph 15, lines 9-16.

Allowable Subject Matter

Claims 6-10 are allowed.

The primary reason for the allowance of claim 6 is the inclusion of the limitations of an access control register setting an access extension time with respect to said external device. It is these limitations found in each of the claims, as they are **claimed in the combination**, that has not been found, taught or suggested by the prior art of record which makes these claims allowable over the prior art.

The primary reason for the allowance of claims 7-10 is the inclusion of the limitations of an access control register setting an access extension time with respect to said external device; an wherein the system LSI comprises a re-map signal generating section which, on the basis of a control signal outputted from the processor, generates a re-map signal, and the control signal specifies said external device when the re-map signal is supplied to the bus interface. It is these limitations found in each of the claims,

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as they are claimed in the combination, that has not been found, taught or suggested by the prior art of record which makes these claims allowable over the prior art.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Demetrius R. Pretlow whose telephone number is (571) 272-2278. The examiner can normally be reached on Mon.-Fri. 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on (571) 272-2269. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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W122 105

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